PATENT CLAIMS

1. A method in the fabrication of an organic thin-film semiconducting device, wherein the semiconducting device comprises an electrode arrangement with electrodes contacting a semiconducting organic material, and wherein the method is characterized by

depositing a first layer of a conducting or semiconducting material or combination of a conducting and a semiconducting material in the form of a patterned or non-patterned layer on an insulating substrate, such that at least a portion of the substrate is covered by the first layer

modifying the work function of the conducting and/or semiconducting material of the first layer by depositing a second layer of a conducting polymer with a work function higher than that of the material in the first layer such that the layer of the conducting polymer mainly covers the first layer or is conformal with the latter, whereby the combination of the first layer and the second layer constitutes the anode of the electrode arrangement and the work function of the anode becomes substantially equal to that of the conducting polymer,

depositing a third layer of a semiconducting organic material on the top of the anode, and optionally and in case only a portion of the substrate is covered by the anode, also above at least some of the portion of the substrate not covered by the anode, and

depositing a patterned or non-patterned fourth layer of a metal on the top of the third layer, whereby the fourth layer constitutes the cathode of the electrode arrangement.

2. A method according to claim 1,
characterized by the conducting material of the first layer being a metal.

3. A method according to claim 2,
characterized by selecting the metal among calcium, manganese, aluminium, nickel, copper or silver.

4. A method according to claim 1,
characterized by selecting the semiconducting material of the first layer among silicon, germanium or gallium arsenide.

5. A method according to claim 1, characterized by depositing the second layer as a dispersion from a dispergent or as a dissolved material from a solution.

6. A method according to claim 1, characterized by depositing the second layer in a melt application process.

7. A method according to claim 1, characterized by selecting the conducting polymer in the second layer on a doped conjugated polymer.

8. A method according to claim 7, characterized by selecting the conjugated polymer among poly(3,4-dioxyethylene thiophene) (PEDOT), a copolymer which includes the monomer, 3,4-dioxyethylene thiophene, substituted poly(thiophenes), substituted poly(pyrroles), substituted poly(anilines) or copolymers thereof.

9. A method according to claim 7, characterized by selecting the dopant for the conjugated polymer as poly(4-styrene sulphonate) (PSS).

10. A method according to ~~claims 7 and 8~~ Claim 7, characterized by selecting as the doped conjugated polymer as poly(3,4-ethylenedioxythiophene) (PEDOT) doped with poly(4-styrene sulphonate) (PSS).

11. A method according to claim 1, characterized by selecting the semiconducting organic material in the third layer among conjugated polymers, or crystalline, polycrystalline, microcrystalline and amorphous organic compounds.

12. A method according to claim 11, characterized by selecting the conjugated polymer in the third layer among poly(2-methoxy, 5-(2'-ethylhexyloxi)-1,4-phenylene vinylene) (MEH-PPV) or poly(3-hexylthiophene) (P3HT).

13. A method according to claim 1, characterized by selecting the metal of the fourth layer among metals which have a lower work function than that of the anode.

14. A method according to claim 13, characterized by selecting the metal of the fourth layer as the same as the metal selected for the first layer.

15. A method according to claim 14, characterized by selecting aluminium as the metal of the fourth layer.

16. Use of the method according to ~~any of the claims 1-15~~ Claim 1 for manufacturing the electrode arrangement in an organic thin-film diode.

17. Use of the method according to ~~any of the claims 1-15~~ Claim 1 for manufacturing the electrode arrangement in a transistor structure, especially in an organic thin-film transistor or a hybrid thin-film transistor.